SUBRANGING ANALOG TO DIGITAL CONVERTER WITH MULTI-PHASE CLOCK TIMING

ABSTRACT OF THE DISCLOSURE

An N-bit analog to digital converter includes a reference ladder, a track-and-hold amplifier connected to an input voltage, a coarse ADC amplifier connected to a coarse capacitor at its input and having a coarse ADC reset switch controlled by a first clock phase of a two-phase clock, a fine ADC amplifier connected to a fine capacitor at its input and having a fine ADC reset switch controlled by a second clock phase of the two-phase clock, a switch matrix that selects a voltage subrange from the reference ladder for use by the fine ADC amplifier based on an output of the coarse ADC amplifier, and wherein the coarse capacitor is charged to a coarse reference ladder voltage during the first clock phase and connected to the T/H output during the second clock phase, wherein the fine capacitor is connected to a voltage subrange during the first clock phase and to the T/H output during the second clock phase, and an encoder that converts outputs of the coarse and fine ADC amplifiers to an N-bit output.